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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/681,068

10/07/2003

Andrew S. Hildebrant

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VERIGY, LTD.

IP LEGAL DEPARTMENT

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CUPERTINO, CA 95014-2540

EXAMINER

LEIVA, FRANK M

ART UNIT

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DELIVERY MODE

05/08/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/681,068	Applicant(s) HILDEBRANT ET AL.	
	Examiner FRANK M. LEIVA	Art Unit 3714	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In view of the Appeal Brief filed on 23 November 2007, PROSECUTION IS HEREBY REOPENED. The New ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Arguments

2. Applicant's arguments, see Appeal Brief, filed 23 November 2007, with respect to 35 U.S.C. §101 Double Patenting, 35 U.S.C §112 and 35 U.S.C. §103 rejections have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of obviousness type provisional double patenting and new art Williams et al. US 2002/0093356 and Ohara et al. US 2002/0143418.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-17 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 and 10-13 of copending Application No. 10/666,024. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the limitations of the rejected claims are claimed in at least one of the claims 1-6 and 10-13 of applicant's copending application, and there is no reason why the rejected claims could not have been presented in the copending application 10/666,024.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US 2002/0093356 A1) in view of Ohara et al. (US 2002/0143418 A1).

7. Regarding the analogous art combination; Williams discloses a method and apparatus for reducing test vector memory and reduce cost of the process; Ohara describes a method and computer product that calculates the total theoretical cost of a project and compares it to the actual cost of the project. The examiner deems obvious to

combine these inventions in order to show the full advantage of Williams invention as to show the current cost versus the new cost after using Williams' invention since it is obvious after reading Williams' invention that cost reduction is the important issue and cost calculation would only be an added predictable programmed feature.

8. **Regarding claims 1, 8 and 13;** Williams discloses a machine-executable method comprising; reading a test file having a plurality of test vectors; determining a required memory needed to execute the plurality of test vectors, (§ [0014]), the method and circuit describes reading and storing the plurality of vectors in memory 1 and analysis the vector data to reduce (determined) the required memory for testing each vector. Williams though speaks of reducing costs by reducing the memory required (based on memory), does not teach of an automated cost estimation. Ohara on the other hand teaches an automated method for calculating project costs which when applied to the Williams invention would use the calculated required memory to estimate a cost to execute the test vectors. Thus, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to apply the technique of calculating the total project cost as taught by Ohara, to improve the final product report of Williams' for the predictable result of generating a reduced vector testing data and a cost reduction comparison between the previous data and testing the new data for sales purposes.

9. **Regarding claim 2;** Williams and Ohara disclose all the limitations of claim 1 from which claim 2 depends on, wherein Ohara also discloses receiving a billing scheme and wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors, (fig. 2), wherein the system receives integrated database information from the target billing report and the actual billing report, wherein as applied above the combined invention of Williams and Ohara would use the memory required to test the vectors to calculate the costs of the project. It would have been obvious to one of ordinary skill to retrieve or receive all of the billing costs used in the project to calculate the total cost.

10. **Regarding claim 3;** Williams discloses determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board, (fig. 3 and ¶ [0046]), wherein the DUT (Device Under Test) is incorporated of several separate circuits such as the LFSR, SEL and IC Block.

11. **Regarding claim 4;** Williams discloses determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin, (¶ [0035]), wherein the circuit calculates the values for every pin and determines the minimum require memory for each pin.

12. **Regarding claim 5;** Williams discloses wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file, (¶ [0057]), wherein Williams acknowledges having multiple tests (test patterns) and having a netlist of all test vectors and patterns (i.e. an accounting or counting of the test vectors).

13. **Regarding claim 6;** Williams discloses determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file; setting the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement, (¶ [0035-0036]), where by determining the random outcome bits and masking them, the system is left with the largest value of deterministic bits to test for, that is, it realizes the largest number of real bits to test for.

14. **Regarding claim 7;** Williams discloses further comprising for each additional test in the test file: for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required

memory, (¶ [0057]), as applied above in claim 5, having to execute several test files, it is obvious that the system will determined all the memory requirements for the additional tests as it does for the first set of test vectors.

15. **Claims 8 & 13:** Rejected under similar rationale as set forth in claim 1.

16. **Claim 9:** Williams as modified by Ohara., discloses further comprising a user interface to display the cost to a user (the examiner views this limitation as since Williams uses a computer, this computer can be used to display the cost; To do so is merely programming and a predictable result of Ohara's sole purpose to generate a costs report.

17. **Claims 10 & 15:** Rejected under similar rational as set forth in claim 3.

18. **Claims 11 & 16:** Rejected under similar rational as set forth in claim 4.

19. **Claim 12:** Rejected under similar rational as set forth in claim 5.

20. **Claim 14:** Rejected under similar rational as set forth in claim 2.

21. **Claim 17:** Rejected under similar rational as set forth in claim 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRANK M. LEIVA whose telephone number is (571)272-2460. The examiner can normally be reached on M-Th 9:30am - 5:pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert E. Pezzuto can be reached on (571) 272-6996. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert E Pezzuto/
Supervisory Patent Examiner, Art Unit 3714

FML 05/05/2008